RFL Electronics Inc.

INSTRUCTION DATA

Model 66A ENC Encoder Controller
and
Model 66A ENC EXP Encoder Expander
HD-44953-JMC-2

PREFATORY NOTE

This data sheet describes Model 66A ENC Encoders and Model 66A ENC EXP Expanders assembled on printed-circuit boards which bear the identification HD-44953-JMC-2 (or higher suffix digits) at the approximate right-center of the component side of the board. These data do not pertain to circuit modules assembled on circuit boards bearing the identification HD-44953-JMC, and those holding such boards should request RFL for a different data sheet, which is available. A statement giving the number appearing on the board of interest will be helpful in filling such requests.

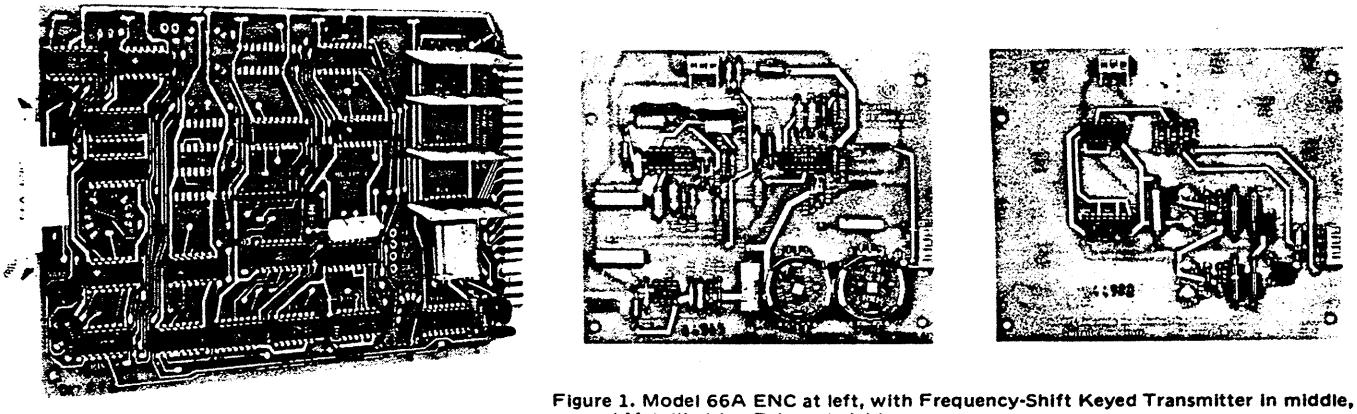

Figure 1. Model 66A ENC at left, with Frequency-Shift Keyed Transmitter in middle, and Metallic-Line Driver at right.

DESCRIPTION

The Model 66A ENC Encoder is one of the logic modules in the RFL Series 6644 Time-Division Multiplex System. It develops a serial-data code representing the status of parallel data-input points. The output data, after transmission over a communication line, are reconstituted at the receiving end by the corresponding decoder card, Model 66A DEC.

An expander card, Model 66A ENC EXP Expander, is available to extend the number of data-input points in increments of 16 points for each expander card.

A block diagram of the circuits of the encoder is shown as Figure 2.

The encoder is designed to key the RFL Model 68B FSTX, or most other voice-frequency carrier-telegraph transmitters, typically as one of a system in which several such transmitters are combined in frequency-division multiplex on a voice-grade communication circuit.

Two optional plug-on cards are availalbe, on special order, for connection to a communication line:

(a) The Model HB-44980 Metallic-Line Driver, which will interface the CMOS output circuits of the encoder to a dedicated two-wire line and also convey information pertaining to change of state by interrupting the communication medium.

(b) The Model HB-44945 FSK V-F Carrier Transmitter which transmits the data with a frequency-shifted audio tone. The output of the transmitter is balanced, nominally 600 ohms, and has a rising impedance out of band to minimize loading of adjacent channels.

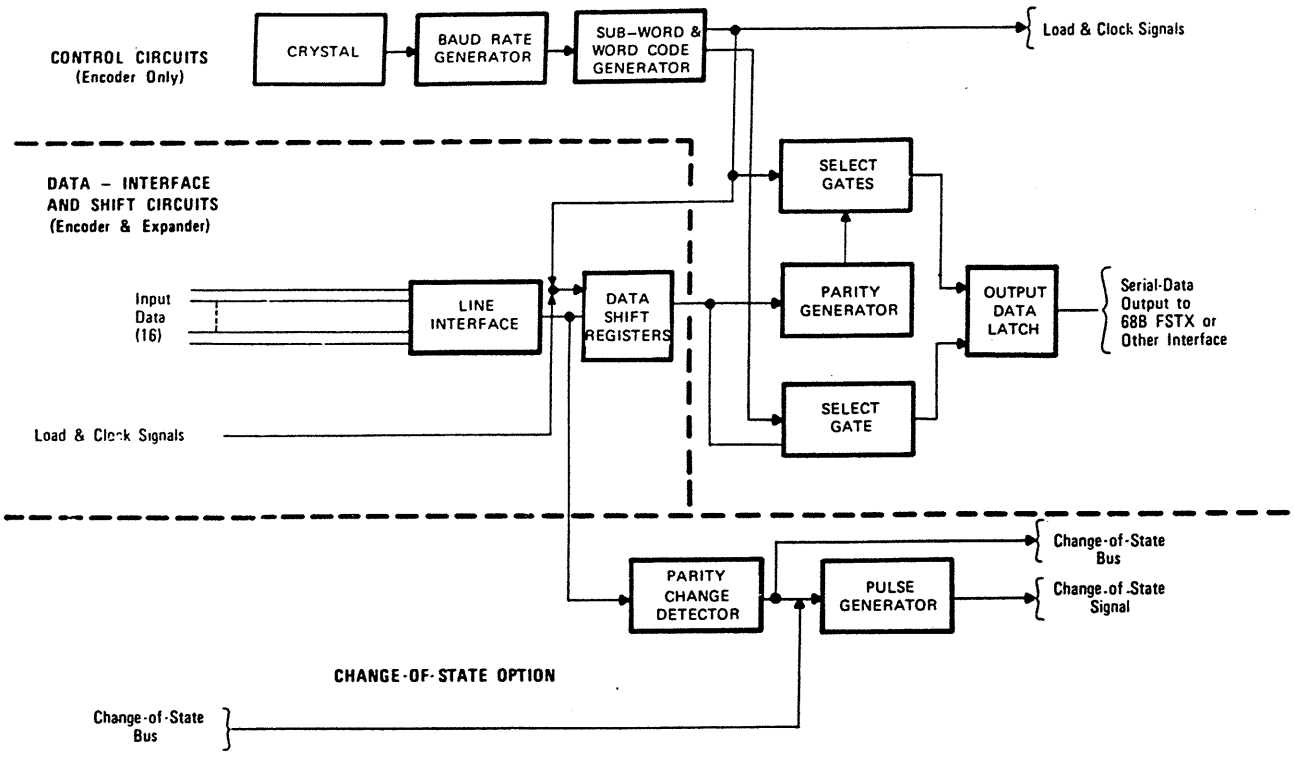

Figure 2. Block diagram of circuits of Model 66A ENC and Model 66A ENC EXP, with change-of-state circuit.

SPECIFICATIONS

Number of Data Bits: Up to 16 data-input points are accepted on the Model 66A ENC. This number may be extended to 32, 48, and 64 bits (double scan), or in multiples of 16 bits to a total of 144 bits (single scan) with the addition of Model 66A ENC-1 Encoder Expanders.

Input: Open collector or contact closure to common (or ground) is standard. Closure to +V is also availalbe.

Data Rates: 60 baud is the standard rate. Rates of 120, 240, or 480 baud are obtained by changing jumpers. Rates to 1600 baud are available on special order.

Code: Each message word begins with a header and contains two parity bits for each 16 data bits. Doublescan is standard; singlescan is optional. Details of the format are shown on Figure 4.

Change-of-State Detector: Option HB-44955, used on Model 66A ENC-2, provides for detection of change of state at input points. Simultaneous changes of input signals occurring within 4 ms of each other will not be detected as a change of state. Option HB-44975 provides the same feature for the Model 66A ENC EXP-3 Expander.

Security: Multiple parity and doublescan are standard. Doublescan can be omitted by changing a jumper.

Time for Scan: At 60 baud with doublescan, a single-word scan requires 1.1 seconds (66 bits). With singlescan the period is 0.57 second (34 bits).

Encoding Indicator: A flashing lamp indicates that the encoder is active.

Model 66A ENC Alone: CMOS-compatible 12-volt pulses suitable for keying RFL Model 68B FSTX or other compatible line-interface unit.

With Optional FS Transmitter HB-44955:

Frequency and Bandwidth: 300 to 3500 Hz center frequency. 120-Hz spacings are standard.

Frequency Tolerance and Drift: ±0.25% over the temperature range.

Output Level: Adjustable from −40 to −3 dBm.

Harmonic Content: Better than 50 dB below fundamental.

Output Impedance: Nominally 600 ohms within the band, with a rising impedance out of band. The two-section output filter is balanced.

With Optional Metallic-Line Driver HB-44980:

Maximum Baud Rate: 600 Baud.

Maximum Total Loop Resistance: 400 ohms.

Operating Ambient-Temperature Range: −30 to 70°C.

Power Requirements: 11 to 13 Vdc, 30 mA, with every input connected to common. Option HB-44945 or HB-44980 each require 10 mA additional. Regulation of 5% or better is required.

Size: Each encoder or extender card occupies two standard one-half-inch module spaces in an RFL Model 68 Chassis. Adding either of the optional, plug-on transmitters causes the Model 66A ENC to occupy three standard one-half-inch module spaces.

ORDERING INFORMATION

A single-card system, with a baud rate of 60 and doublescan, is standard. Other choices are available, in which case the desired operating baud rate must be specified from Table 1, and the desired message format must be stated from Table 2. Specific Model designations for standard models are given in the accompanying table.

SERIES 66 TDMS MODEL 66A ENCODERS	Encoder HB-44950	Change-of-State Detector HB-44955	Encoder Expander HB-44970	Change-of-State Detector HB-44975	Modification for FS Trans. $10.00	44945 $130.00 FS Trans. Opt.
66A ENC	•					
66A ENC EXP-1			•			
66A ENC-2	•	•				
66A ENC EXP-3			•	•		
66A ENC-4	•				•	•
66A ENC-5	•	•			•	•
APPLICABLE CONNECTOR ASSEMBLY	HB-90483					

The FSK transmitter or the metallic-line driver are available on special order.

A connector wiring assembly is available for easy field wiring of this module into a properly equipped RFL Model 68 Chassis. When this connector assembly is used, the number of status points available is eight. The external chassis wiring is shown in Figure 3.

Connections shown below apply when the specified connector assembly is used. When chassis are completely wired by RFL, a connection diagram is furnished.

Note: Only 8 outputs are available when the connector assembly is used.

The uncircled number shown at the right indicates the data position in the serial pulse code, and corresponds to the respective input and output points of encoders and decoders.

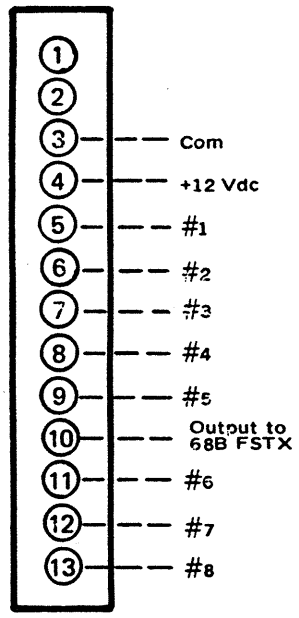

Figure 3. Terminal assignments for connector wiring assembly.

CODE FORMAT

Each word is made from four subwords, and each word is comprised of the serial data generated by one encoder card.

The first subword is an unique ten-bit stream of ten logic lows which synchronize the system. Each of the remaining three subwords carries data bits, while the fourth and final subword also carries two parity bits which indicate the two least-significant bits of the binary sum of all high data bits for the entire word.

Each message may contain one or more words. They use the same format as the first word except that the first subword contains all logic highs, is not unique to the system, and so can not be confused as a header signifying the beginning of a message.

The message used for doublescan consists of word sequences transmitted twice. The word header of the second scan, however, consists of highs, and the subwords will be inverted on the second transmission.

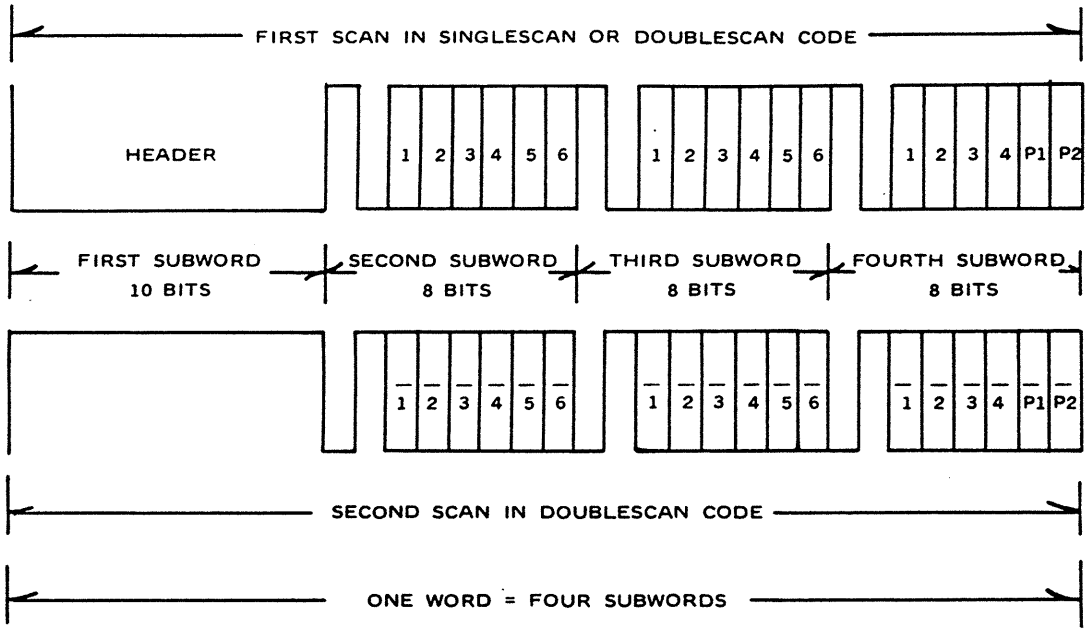

Figure 4. Code format used for Model 66A DEC.

PROGRAMMING AND CONNECTIONS

All semiconductors, and especially smaller ones such as small-signal transistors, linear and digital integrated circuits, and microprocessors, are vulnerable to the possibility of damage from static charges. Procedures for minimizing this possibility are outlined in RFL Document 12175A.

All unused input terminals should be returned to +V or to circuit common, according to the function required.

Circuit

The logic card is divided into three sections, as shown on Figure 8: (a) the Circuit-Controls Section, (b) a Data-Interface and Shift Section, and (c) an optional Change-of-State Section. The Model 66A ENC uses (a) and (b), with (c) available as an option. The Model 66A ENC EXP Encoder Expander requires (b), and (c) is available as an option.

Baud Rate

The baud rate of the Model 66A ENC is set at the factory. It is determined by selecting a quartz crystal of the appropriate frequency and by installing jumpers as shown in Table 1.

TABLE 1

BAUD-RATE PROGRAMMING & CRYSTAL OPTIONS

Baud Rate	Suffix to Crystal's P/N HB-37440-(**)	Crystal Freq. MHz	BAUD Jumper
1600	-51	3.2768	F
1280	-99	2.6214	E
1200	-97	2.4576	F
1120	-98	2.2938	F
960	-53	3.9321	E
800	-51	3.2768	E
640	-99	2.6214	E
600	-97	2.4576	E
560	-98	2.2938	E
480	-53	3.9321	D
400	-51	3.2768	D
320	-99	2.6214	D
300	-97	2.4576	D
280	-98	2.2938	D
240	-53	3.9321	C
200	-51	3.2768	C
160	-99	2.6214	C
150	-97	2.4576	C
140	-98	2.2938	C
120	-53	3.9321	B
100	-51	3.2768	B
80	-99	2.6214	B
75	-97	2.4576	B
70	-98	2.2938	B
60	-53	3.9321	A*
50	-51	3.2768	A
40	-99	2.6214	A
35	-98	2.2938	A

*Denotes standard model.

Message Length

Each message contains one or more words, and each word contains sixteen data bits as well as the associated control bits. Table 2 shows the jumpers to be selected for messages of different lengths and scans.

Intraboard and Interboard Wiring

The intraboard wiring of a one-word-message encoder is treated in the same manner as is the interwiring of a multi-word message-encoder system. For message-length expansion, Model 66A ENC EXP Cards are connected in series with a Model 66A ENC Control Card. **The control card must be positioned to provide the final serial-data** output to the communication line.

For serially connected cards, each EXTENDER OUT, Terminal 22, is connected to the succeeding encoder's SERIAL-DATA INPUT, Terminal S. For all applications, the 66A ENC control encoder card's $\overline{\text{EXTENDER OUT}}$, Terminal N, is connected to the initial or single-word encoder card's SERIAL-DATA INPUT, Terminal S.

TABLE 2

MESSAGE-LENGTH PROGRAMMING

Message Length (in words)	SCAN Number	WORD Jumper
1	Single	1
1	Double	2 *
2	Single	2
2	Double	4
3	Single	3
3	Double	6
4	Single	4
4	Double	8
5	Single	5
6	Single	6
7	Single	7
8	Single	8
9	Single	9

LOAD CLOCK, Terminal R, of each interconnected encoder must be connected. Similarly, the SHIFT CLOCK, Terminal P, must also be interconnected among all cards.

The INITIALIZATION signal, Terminal L, may be used to initialize circuits requiring power-up initialization.

Data-Encode Control

When Jumper PI is selected, the encoder will encode data whenever PULSE INITIATE, Terminal M, is held high or open. Selection of Jumper CK will enable the encoder to transmit a single valid message each time a positive single transition is applied to CLOCK INITIATE, Terminal K.

Data-Outputs

The 66A ENC Control Encoder's SERIAL-DATA OUTPUT, Terminal 21, will be connected to a CMOS-input compatible line-interface device. If either the Metallic-Line Driver, Option HB-44980, or the FS Transmitter, Option HB-44945, is used, the HIGH and LOW OUTPUTS, Terminals X and 20, are connected to the compatible lines, and the SERIAL-DATA OUTPUT remains unconnected.

The DATA-LOADED signal, Terminal Y, develops a positive pulse after the data have been internally latched into the encoder. This signal can be used for updating A/D converter outputs.

Data Inputs

Input connections appear at the left side of Figure 8. The sixteen inputs are normally high and interface with either contact-closure or open-collector inputs. For inputs using closure to signal common, use the jumper to +V. For inputs using closure to +V, use the jumper to common.

Change of State

The Change-of-State option is identified as Assembly HB-44955 for the Model 66A ENC, and as Assembly HB-44975 for the Model 66A ENC EXP.

The control encoder's $\overline{\text{CARRIER ON}}$ signal, Terminal V, or its CARRIER ON indicator at Terminal U, develops an output for at least a single scan after a change of state is detected. When the change-of-state option is used, all series-connected encoder card's EXPANDED CHANGE-OF-STATE signals, Terminal T, must be interconnected. Note that simultaneous changes in input signals occurring within 4 ms of each other will not be detected. On special order, this time can be reduced to 1 ms.

When change-of-state data are to be transmitted as data, CARRIER ON, Terminal U, or $\overline{\text{CARRIER ON}}$, Terminal V, must be connected to INPUT 1, Terminal 3, and Jumper CS (located near IC3) must be employed. For all other conditions, Jumper CR is used and all sixteen inputs are available for input data.

FS Transmitter, Option HB-44945

Input Data

Modulation is applied to the transmitter through DATA INPUT, Terminal DA. When this transmitter is used with the Model 66A ENC, Jumper J2, Figure 6, should be in place.

Change-of-State Detection

When change-of-state detection is not used, Jumper A, Figure 6, is used to keep gate IC2B closed. When a change of state is to be communicated by interruption of the carrier, Jumper B is used.

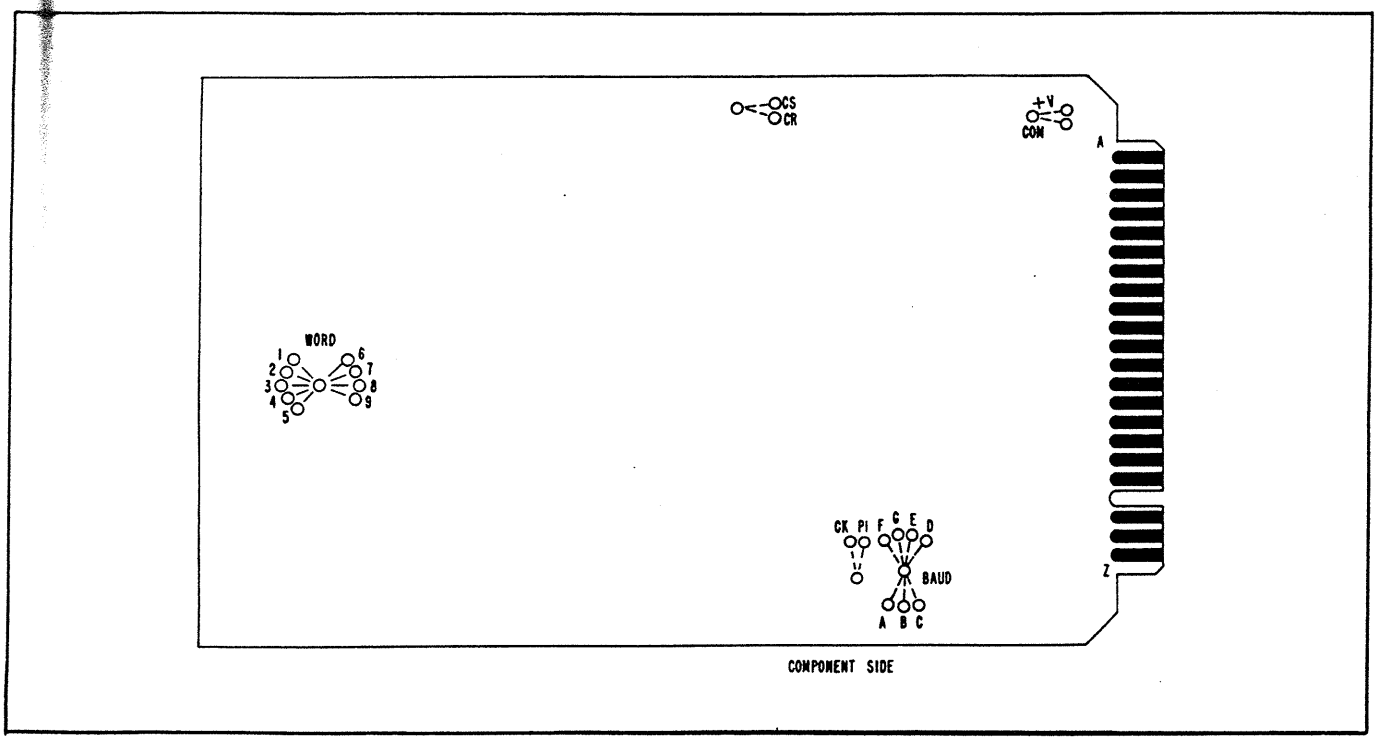

Figure 5. Location of jumpers, Model 66A ENC and Model 66A ENC EXP.

Adjustments

Frequency Adjustment

Connect a frequency counter between TP1 and COM. Key the transmitter to both high and low frequencies and measure. The two frequencies need not be exact, but they should be symmetrical with respect to the center frequency of the channel. Make adjustment with FREQ, R13, Figure 6, which changes both frequencies in the same direction.

Level Adjustment

The output level is adjustable with LEVEL potentiometer, R24, between −40 and −3 dBm. Adjust R24 for the required level on the line, using a high-impedance ac voltmeter, by terminating the transmitter with a 600-ohm resistor or with all other parallel-connected transmitters on the line not operating.

After all transmitters are adjusted and operating, measure and record the output level of each between TP1 and

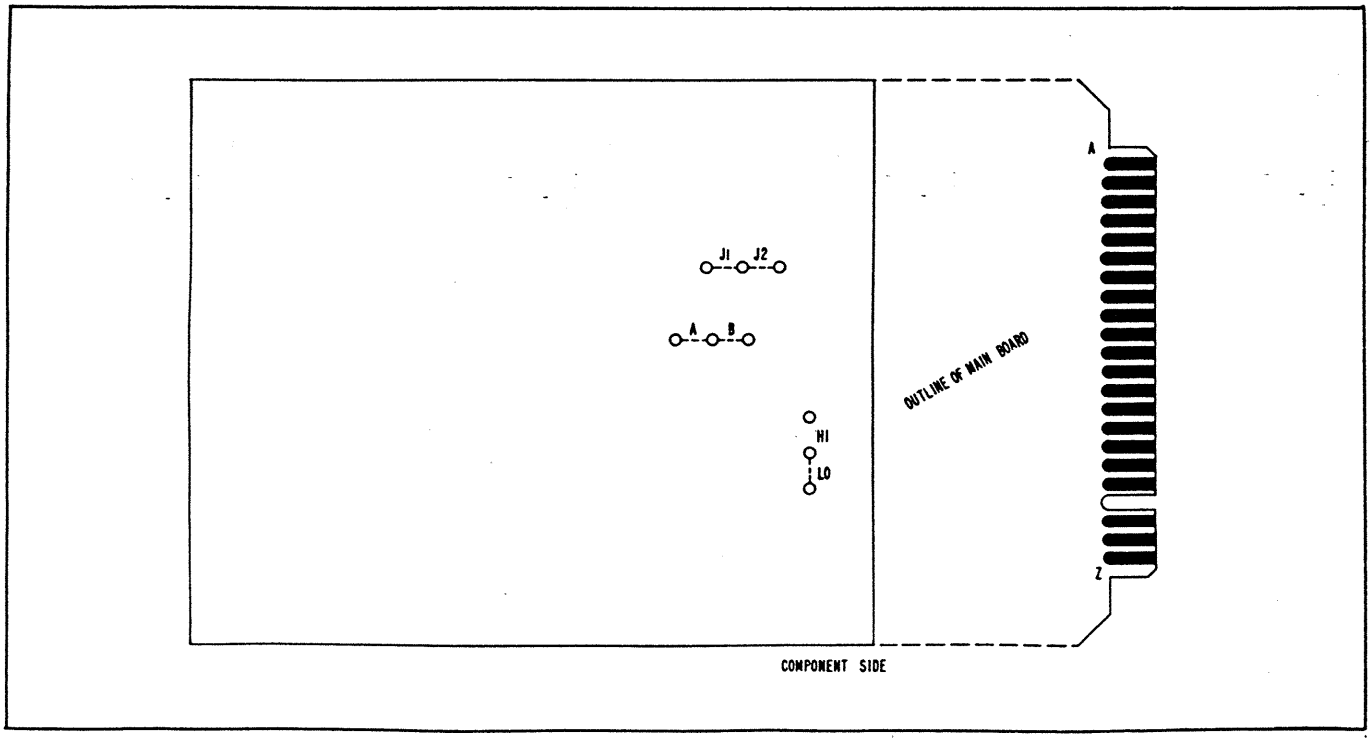

Figure 6. Location of jumpers, FS Transmitter, Option HB-44945.

COM. The voltage readings will be different from the reading obtained across the line. They can be used for future reference.

Metallic-Line Driver, Option HB-44980

Jumper AB, Figure 7, is used when a signal from the change-of-state detector is used to interrupt the communication process. For continuous communication, Jumper AC is used.

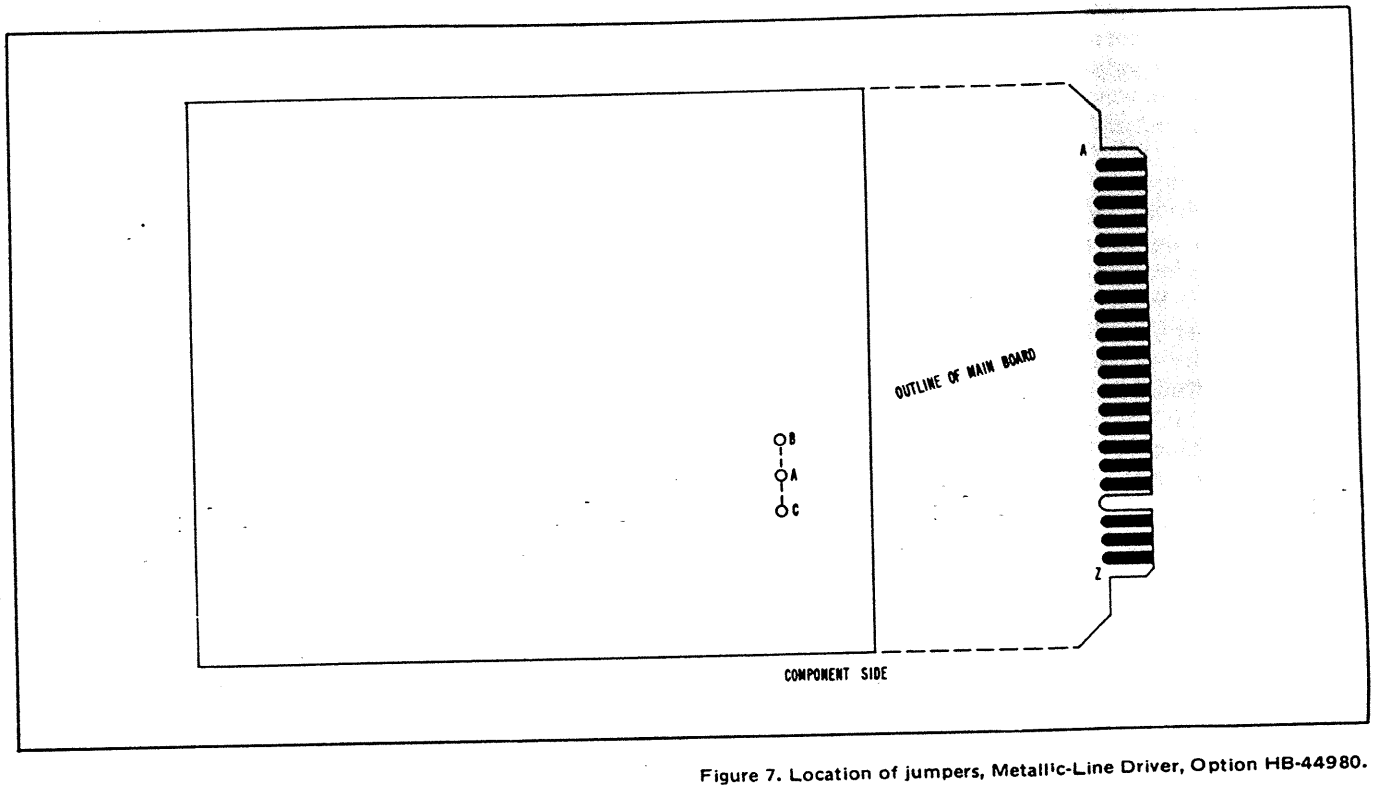

Figure 7. Location of jumpers, Metallic-Line Driver, Option HB-44980.

CIRCUIT THEORY

Data Latch and Shifting

Data at the input lines are latched into parallel-to-serial shift registers, IC4, IC7, and IC8, Figure 8, during the positive LOAD CLOCK signal at Pin 9 of all three registers. Input lines are buffered by resistance-capacitance networks RC1, RC2, RC3, and RC4. Jumper +V causes the pull-up resistors to hold the inputs high when not forced to circuit common. The latched data are serially shifted through the shift registers by the SHIFT CLOCK signal at Pin 10 of all three registers, and the data exits at Pin 3 of IC4. Data are then shifted through IC1A-1, inverted and buffered by IC13-4 and developed at SERIAL DATA OUTPUT, Terminal 21.

Data from series-connected Model 66A ENC Encoder Extender cards may be shifted into the succeeding register group through SERIAL-DATA INPUT, Terminal S, and out of the group through EXTENDER OUT and $\overline{\text{EXTENDER OUT}}$, Terminals 22 and N, respectively.

Circuit-Controls Section

The circuit-controls section uses several counters. IC19, the baud-rate counter, develops a clock signal proportional to the number of bits shifted by the system. The basic shift-register-clock signal appears at IC17-11, from where it is gated through IC15-3 during the non-header phase. Data will be shifted during the second, third, and fourth subwords of the basic data word shown in Figure 4. IC4 contains the second subword, IC8 the third, and IC7 the fourth.

Initializing the Circuit

When power is first applied, C4 is charged through R6 and this will cause a momentary high to appear at IC13-12. This signal directly initializes both the baud-rate counter, IC19, and the bit-rate counter, IC17. Indirectly, it also initializes the subword and word counters, IC5 and IC9, through their reset inputs at Pin 15.

Data-Shift Clocking

Pin 6 of IC13 provides the driver and inverter for the crystal-oscillator circuit which generates the basic clock pulse used to establish the baud rate of the system.

The clock signal clocks the baud-rate counter at IC19-10. This develops the basic baud rate, which then clocks the bit-rate counter at IC17-1. IC17-11 generates the shift-register-clock signal.

After each set of eight data bits has been shifted, the bit-rate counter causes the subword counter, IC5, to be incremented with a clock pulse to IC5-13. Each subword is designated by the output pattern of the subword counter, IC5. An output at either Pin 2 or Pin 11 indicates the existence of the header for the message. For every shifting of two words, the output of IC2D-11, causes an incrementation of the word counter, at IC9-14. An output at the word jumper, corresponding to the completion of transmission of the required word, will then cause the generation of a new header by applying a signal to IC14B-11.

The output of flip-flop IC1B-13 determines the initial header. This output forces the serial-data output of flip-flop IC1A-1 high during the initial header. The header flip-flop, IC1B, is reset by the subword indicator "1" signal from IC5-1. Succeeding subheaders force IC1A-1 low through a reset signal from IC2D-11. Subwords 2, 3, and 4 may now be shifted out of the serial-data-output flip-flop, IC1A-1. This shifting is accomplished through the clock signal at IC11-3, which is generated by the output of the bit-rate counter, IC17-11, and by the non-header-indicator output from IC2D-11.

As the data are shifted, the parity is totalized by the flip-flop combination IC18A and IC18B, wired as a standard binary-counter combination. The timing-window signals from Pins 11 and 12 of bit-rate counter IC17, and the serial data from the shift register's outputs generate the clock signal to the parity totalizer. This totalizer is reset by the header-indicator signal at IC2D-11. The parity data are injected into the data stream through IC16D-10 during the last two bit frames in the last subword of each word in the message. Placement of the parity bits into the data stream is controlled by Gates 10 of IC15C and 4 of IC11B. The gating is controlled by timing signals from the bit-rate counter, IC17, and by the subword-indicator output from IC5. The resultant signal window indicates the existence of the seventh and eighth bits in the final subword of each message word.

For doublescan, the output of the inverting gate, IC3D-10, is looped back into the SERIAL-DATA INPUT at Terminal S. Data are then recycled and inverted simultaneously.

Circuit-Control Section

The encoder operates in a continuous, cyclic manner if the pulse input, Terminal M, is held high or open and Jumper PI is selected. This will cause a low to IC14B-10, from IC20A-2, and will enable normal continuous coding. If Jumper CK is used, a positive transistion to the clock input, Terminal K, will cause a single pulse from IC20B to initiate a single encode message transmission through IC20A and a low at IC14B-10. Succeeding encode transmissions are disabled by a high to IC14B-10, generated by a clock signal to IC20A-3.

The circuit is initiated by a clock signal to flip-flop IC14B-11, or by a power-up reset signal from IC13E-12 to IC14B-10, which will cause the encoder to initiate a data-load serial-shift sequence. The status of flip-flop IC14B will now allow IC11C-10 to deliver a load pulse to shift registers IC4, IC7, and IC8. This pulse causes the register to latch the parallel input data.

The load pulse will cease when the second bit of the initial header has been transmitted. This occurs when IC14A-2 is toggled by a clock input at Pin 3 from bit-counter IC17. This toggling also causes generation of the DATA LOADED pulse through IC16B-6, and it also causes reset of bit-rate counter IC17 from IC14A-2. IC14B-13 is then toggled, again through IC15B-4, with an enable signal from the baud-rate counter, IC19. Once flip-flop IC14B-13 is again toggled, the reset signal is removed from the subword and word counters, IC5 and IC9, through a low at IC14B-12. After this point, all counters are free to increment again, providing continuous operation is enabled by the state of the flip-flops of IC20.

Change-of-State Detectors, Options HB-44955 and HB-44975

Each input signal is tied to the input of an EXCL-OR gate. The resultant parity tree, consisting of IC3 and most of IC6, generates a transistion signal each time the state of any input changes in either direction. This transition, from IC3-9, is filtered by R4 and C2. If the resulting translated signal is longer than 3 ms, then the dissimilar signals at IC6D-12 and -13 will cause an output pulse at IC6D-11. This pulse will momentarily reset the binary-counter combination IC10A and IC10B. The input-clock source to Pins 3 and 11 of IC10 will then cause flip-flop-output toggling until it develops an output at IC10A-1.

During this counting period, change-of-state indicator signals will be developed at CARRIER ON and at $\overline{\text{CARRIER ON}}$, Terminals U and V, respectively. The change-of-state indicator, EXPANDED CHANGE-OF-STATE, Terminal T, will be driven high. The final output will cause the clock input at IC2C-10 to be disabled. The change-of-state indication will remain for one or two message transmissions.

For serially connected encoders and expanders, the EXPANDED CHANGE-OF-STATE output/input line, Terminal T, will act as a bus line for the several change-of-state circuits.

FS Transmitter, Option HB-44945 Active-Filter Oscillator

Figure 9 is the schematic of the circuit of the FS transmitter. Operational amplifiers IC1A, IC1C, and IC1D, with associated passive components, form a high-Q bandpass filter. IC1C and IC1D are identical integrators connected in series and with their output fed back to the input through inverting amplifier IC1A. The resonant frequency of the filter is controlled by the time constant of the integrators and the gain of IC1A. The gain-adjustment potentiometer, R13, FREQ, enables frequency trimming. The filter is made to oscillate by feedback from IC1C through inverting amplifier IC1B and R15 to the non-inverting input of IC1A. Limiting in IC1B stabilizes the sinewave output of IC1C to approximately 1 volt peak.

The frequency of the oscillator is shifted by switching shunt resistors across the driving resistance of each integrator. IC2A and IC2C are FET bilateral switches controlled simultaneously by logic signals. The filter oscillates at the low frequency when the switches are open, and it will shift to a higher frequency when the switches are closed.

Data-Input Circuit

The incoming data are fed through DATA INPUT, Terminal DA. The keying switches, IC2A and IC2D, can be driven directly with the incoming data through Jumper J2. They can also be driven by the complement of this signal through switch IC2C and Jumper J1.

Change-of-State Detection

When a change-of-state detector is not used, Jumper A is used to keep the control input of IC2B high in order to maintain a closed gate. When change of state is to be communicated by loss of carrier, COS-DETECTOR INPUT, Terminal CE, is brought low, and through Jumper B the signal is disabled.

Output Amplifier

Operational amplifier IC3 is connected in the non-inverting mode. Input resistor R25, and feedback resistor R26 stabilize the gain. Signals from the oscillator are gated by IC2B to the level-control potentiometer, R24, OUTPUT LEVEL, which returns to the +V/2 bus. The output of IC3 is coupled through C10 into a two-section bandpass filter, which connects to a two-wire line with a balanced output.

Metallic-Line Driver, Option HB-44980

When DATA INPUT, Terminal DA, Figure 10, is at a logic high, the output of IC1A is driven low. This causes the outputs of IC2A, IC2B, and IC2C to become high. Q1 conducts and output-line HI goes to a logic high.

Simultaneously, the input of IC1B is high, and the input of IC1D is high because Jumper AC is assumed to be in place. Their outputs are low, so that IC2C-10 is high. This drives the outputs of IC2D, IC2E, and IC2F low to cause Q4 to conduct so that output-line LO goes low.

Conversely, the status of the HI and LO output lines will reverse when DATA INPUT is low.

If Jumper AB is used, and if the COS-DETECTOR INPUT, Terminal CE, goes low, both HI and LO output lines will go high, irrespective of any signal that may be present on the DATA INPUT line. This signals a change of state by interrupting the communication circuit.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 66A ENC Encoder Controller, Assembly HB-44950	
C1	Capacitor, tantalum, 4.7µF, 20%, 20V, Kemet T324B475M020AS, or eq.	H-1007-711
C2	Capacitor, metallized polycarbonate, 0.47µF, 2%, 100V, Wesco 32MPC, or eq.	H-1007-971
C3	Capacitor, metallized polycarbonate, 0.1µF, 2%, 200V, Wesco 32MPC, or eq.	H-1007-962
C4	Capacitor, MPC, 0.47µF, 2%, 100V, Wesco 32MPC, or eq.	H-1007-971
C5, 7	Capacitor, dipped-mica, 390pF, 5%, 100V, Electromotive DM-10, or eq.	H-1080-379
C6	Capacitor, dipped-mica, 150pF, 5%, 500V, Electromotive DM-15, or eq.	H-16516
C8	Capacitor, dipped-mica, 39pF, 5%, 100V, Electromotive DM-10, or eq.	H-1080-385
C9	Capacitor, dipped-mica, 100pF, 5%, 500V, Electromotive DM-15 or eq.	H-1080-338
C10, 11, 12	Capacitor, ceramic, 0.1µF, 10%, 50V	H-0130-51041
CR1, CR2	Diode, silicon Type 1N914B/1N4448	HA-26482
DS1	Lamp, LED, Dialight 550-0102, or eq.	HA-39568
IC1, 14, 18, 20	Dual, D-type flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC2, 12	Quad, 2-input OR gate, RCA CD4071BE, or eq.	H-0615-24
IC3	12-bit parity tree, Motorola MC14531BCP, or eq.	H-0615-72
IC4, 7, 8	Eight-stage static shift register, RCA CD4021AE, or eq.	H-0615-36
IC5	Divide-by-eight Counter/Divider, RCA CD4022AE, or eq.	H-0615-6
IC6	Quad EXCL-OR gate, Motorola MC14070BCP, or eq.	H-0615-69
IC9	Decade counter/divider, RCA CD4017AE, or eq.	H-0615-38

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
IC10	Dual D-type flip-flop, RCA CD401 3AE, or eq.	H-0615-1
IC11	Quad, 2-input NOR gate, RCA CD4001 AE, or eq.	H-0615-3
IC13	Hex inverting buffer, Harris CD4049UBE or Motorola MC14049UBCP	H-0615-7
IC15	Quad, 2-input AND gate, RCA CD4081BE, or eq.	H-0615-31
IC16	Triple, 3-input, AND gate,	H-0615-32
IC17	Seven-stage binary counter RCA CD4024AE, or eq.	H-0615-14
IC19	14-stage binary counter, National CD4020BMJ	H-0615-208
R1-10	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
R11	Resistor, metal film, 1%, 1/4W, 75 ohm	H-0410-1180
RC1	Resistor, capacitor network, RFL HB-471168 only	HB-47168
RZ1	Resistor network, metal-film, 47K, 2%, 2.7 w/pkg., Beckman 785-1-R47K, or eq.	HA-49511
Y1	Piezoelectric crystal, frequency as specified	HA-37440-(xx)
...	Bar, shorting, single	HA-42904
...	Schematic (Figure 8)	HE-44954
	Change-of-State Detector, Option HB-44955	
C1	Not used	
C2	Capacitor, MPC, 0.47μF, 2%, 100V, Wesco 32MPC, or eq.	H-1007-971
C3	Capacitor, MPC, 0.1μF, 2%, 100V, Wesco 32MPC, or eq.	H-1007-962
CR1	Diode, silicon Type 1N914B/1N4448	HA-26482
IC1, 2	Not used	
IC3	12-bit parity tree, Motorola MC14531BCP, or eq.	H-0615-72
IC4, 5	Not used	
IC6	Quad, EXCL-OR gate, Motorola MC14070BCP, or eq.	H-0615-69
IC7 - 9	Not used	
IC10	Dual, D-type flip-flop, RCA CD4013AE, or eq.	H-0615-1
R1, 2, 3	Not used	
R4, 5	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
	Model 66A ENC Encoder Expander, Assembly HB-44970	
C1	Capacitor, tantalum, 4.7μF, 20%, 20V, Kemet T324B475M020AS, or eq.	H-1007-711
C2	Capacitor, metallized polycarbonate, 0.47μF, 2%, 100V, Wesco 32 MPC, or eq.	H-1007-971
C3	Capacitor, metallized polycarbonate, 0.1μF, 2%, 200V, Wesco 32 MPC, or eq.	H-1007-962
CR1	Diode, silicon, Type 1N914B/1N4448	HA-26482
IC3	12-bit parity tree, Motorola MC14531BCP, or eq.	H-0615-72
IC4, 7, 8	Eight-stage static shift register, RCA CD4021AE, or eq.	H-0615-36
IC5	Not used	
IC6	Quad EXCL-OR gate, Motorola MC14070BCP, or eq.	H-0615-69
R1, 4, 5	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
R2, 3	Not used	
RC1 - 4	Resistor, capacitor network, RFL HB-47168 only	HB-47168
RZ1	Resistor network, metal-film, 47K, 2%, 2.7w/pkg., Beckman 785-1-R47K, or eq.	HA-49511

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Change-of-State Detector, Option HB-44975	
C1	Not used	
C2	Capacitor, MPC, 0.47μF, 2%, 100V, Wesco 32MPC, or eq.	H-1007-971
C3	Capacitor, MPC 0.1μF, 2%, 100V, Wesco 32MPC, or eq.	H-1007-962
CR1	Diode, silicon, Type 1N914B/1N4448	HA-26482
IC1, 2	Not used	
IC3	Twelve-bit parity tree, Motorola MC14531BCP, or eq.	H-0615-72
IC4, 5	Not used	
IC6	Quad, EXCL-OR gate, Motorola	H-0615-69
R1, 2, 3	Not used	
R4	Resistor, fixed, composition, 100K, 5%, 1/4W, Allen Bradley CB, or eq.	H-1009-795
R5	Resistor, fixed, composition, 30K, 5%, 1/4W, Allen Bradley CB, or eq.	H-1009-888
	Frequency-Shift Transmitter, Option HB-44945	
C1	Capacitor, tantalum, 33μF, 20%, 10V, Kemet T324D336M010AS, or eq.	H-1007-653
C2, 3	Values are frequency-dependent	
C4 - 7	Capacitor, tantalum, 2.2μF, 20%, 25V, Kemet T324B225M025AS	H-1007-645
C8, 9	Values are frequency-dependent	
C10	Capacitor, tantalum, 15μF, 20%, 20V, Kemet T324B156M020AS, or eq.	H-1007-716
IC1	Quad, linear opamp, Raytheon RC4136NB, or eq.	H-0620-149
IC2	Quad, bilateral switch, Fairchild F4066PC only	H-0615-65
IC3	Linear opamp, RC4131NB	H-0620-133
L1	Value is frequency-dependent	
R1, 2, 3, 14, 15, 16, 17, 20, 25, 26, 28	Resistor, metal film, 1%, 1/8W, value on schematic, Type RN55D, RFL Spec HA-38301	H-1510-(xxx)
R4, 5, 11, 12, 16, 18, 19, 22, 23, 27	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
R6-10, 21	Value is frequency-dependent	
R13	Resistor, variable metal-film, 1K, 10%, 0.75W, Beckman 79PR1K, or eq.	HA-39574
R16	Not used	
R24	Resistor, variable, metal-film, 10K, 10%, 0.75W, Beckman 79PR10K, or eq.	HA-39539
———	Bar, shorting, single	HA-42904
———	Schematic (Figure 9)	HC-44949
	Metallic-Line Driver, Option HB-44980	
C1	Capacitor, tantalum, 47μF, 20%, 20V, Corning CCZ-020-476-20	HB-1007-889
CR1, 2, 4, 5	Diode, Type 1N4001	HA-38876
CR3, 6	Varistor, 15.2–16.8 bipolar breakdown, Gen. Semiconductor, Indus. 1.5KE16CA	HA-44982
IC1	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC2q	Hex inverter buffer, RCA CD4049AE, or eq.	H-0615-7
Q1, 3	Transistor, silicon, NPN, Type 2N2222A	HA-37445
Q2, 4	Transistor, silicon, PNP, Type 2N2907A	HA-37439

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
R1, 2	Resistor, fixed, composition, 100 ohms, 1W, 10%, Allen Bradley GB, or eq.	H-1009-200
R3, 4	Resistor, fixed, composition, 100K, 5%, 1/4W, Allen Bradley CB, or eq.	H-1009-795
R5, 6	Resistor, fixed, composition, 10K, 5%, 1/4W, Allen Bradley CB, or eq.	H-1009-742
RT1, 2	Thermistor 47 ohms, 20%, 125V, Murata PTH61AR470M2B151, or eq.	HA-41942
---	Schematic (Figure 10)	HC-44984

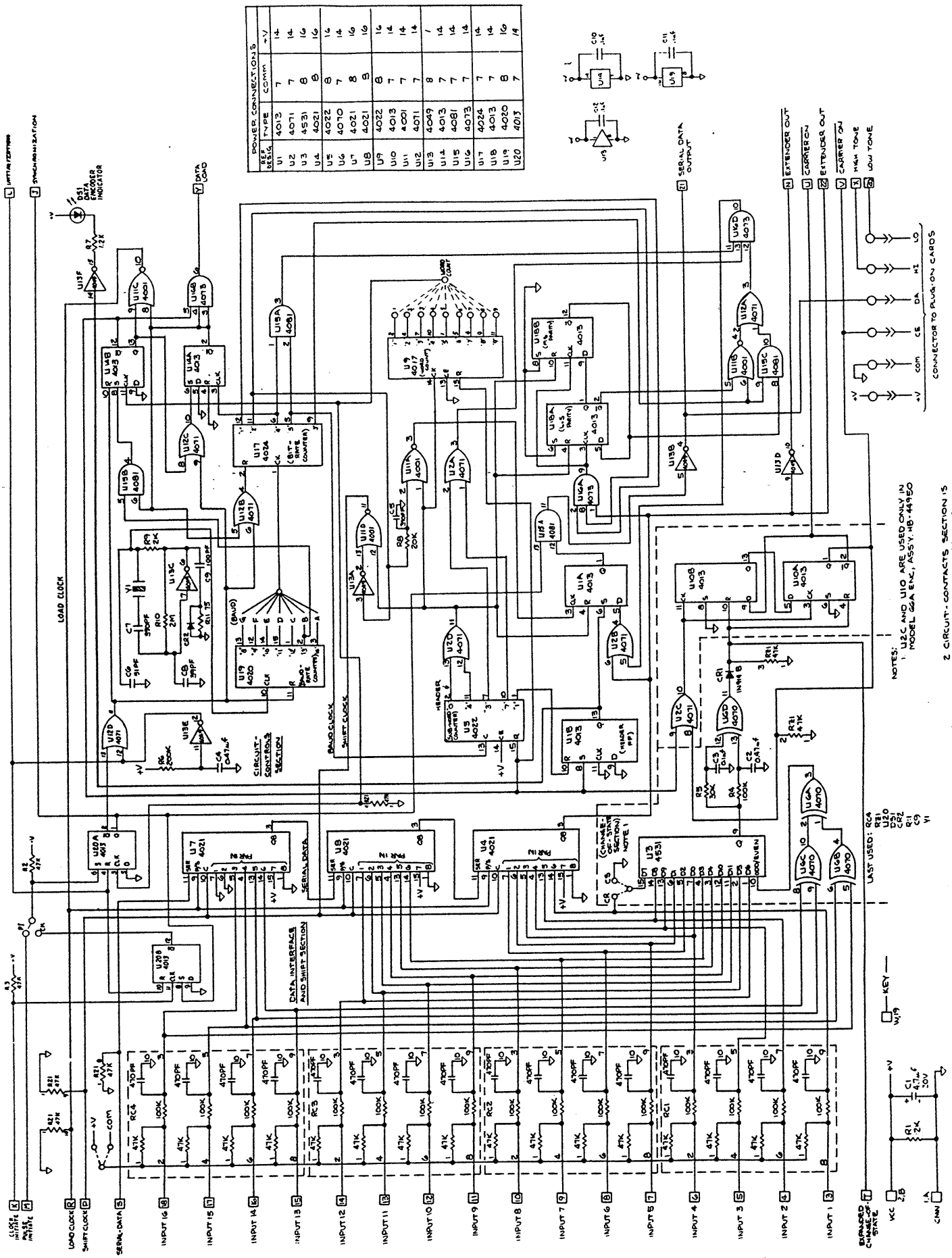

Figure 8. Schematic of circuit, Models 66A ENC and 66A ENC EXP. For the expander card, the circuit-controls section is omitted. Change-of-state section is optional on both models.

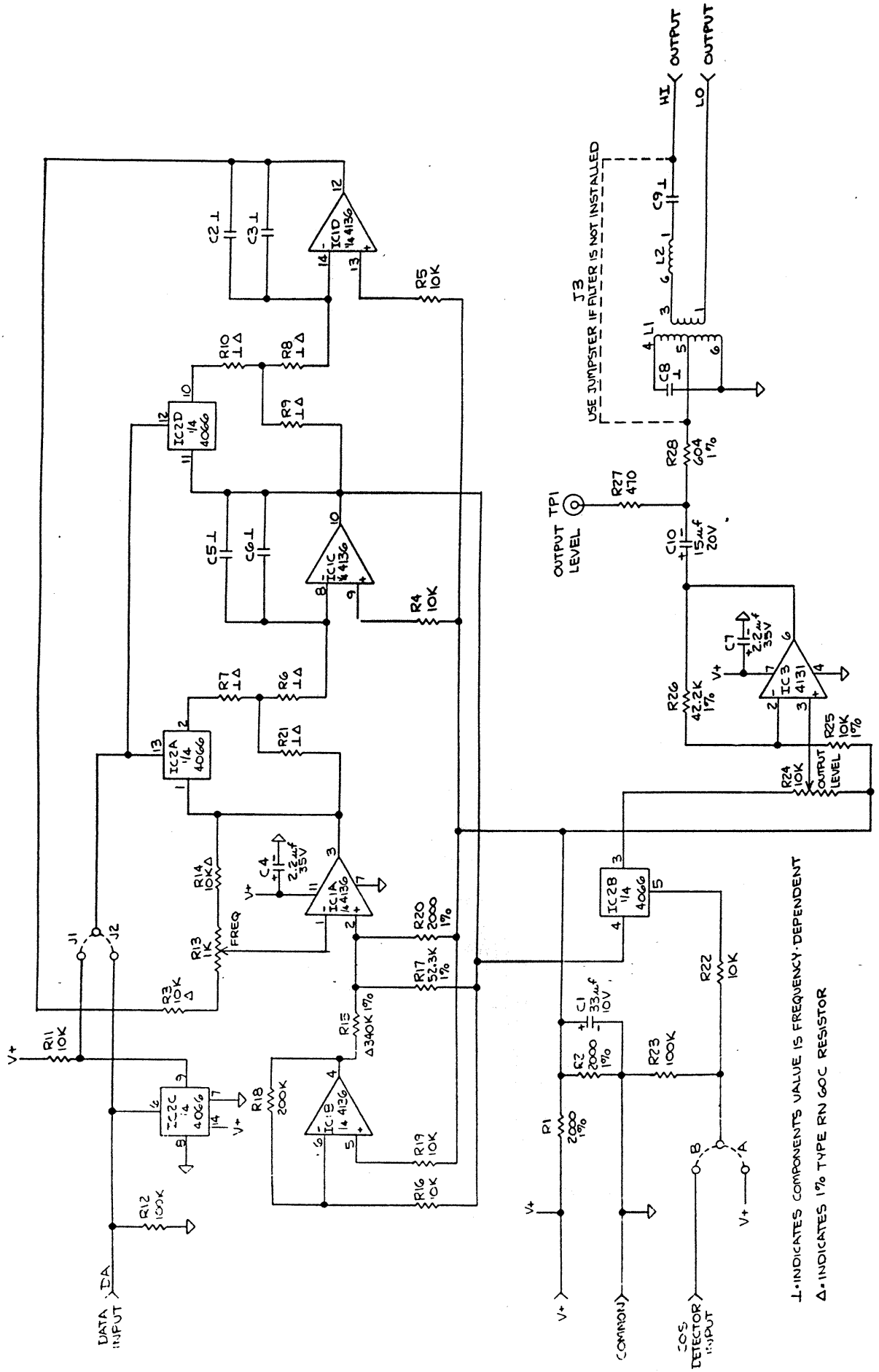

Figure 9. Schematic of circuit for FS Transmitter, Option HB-44945.

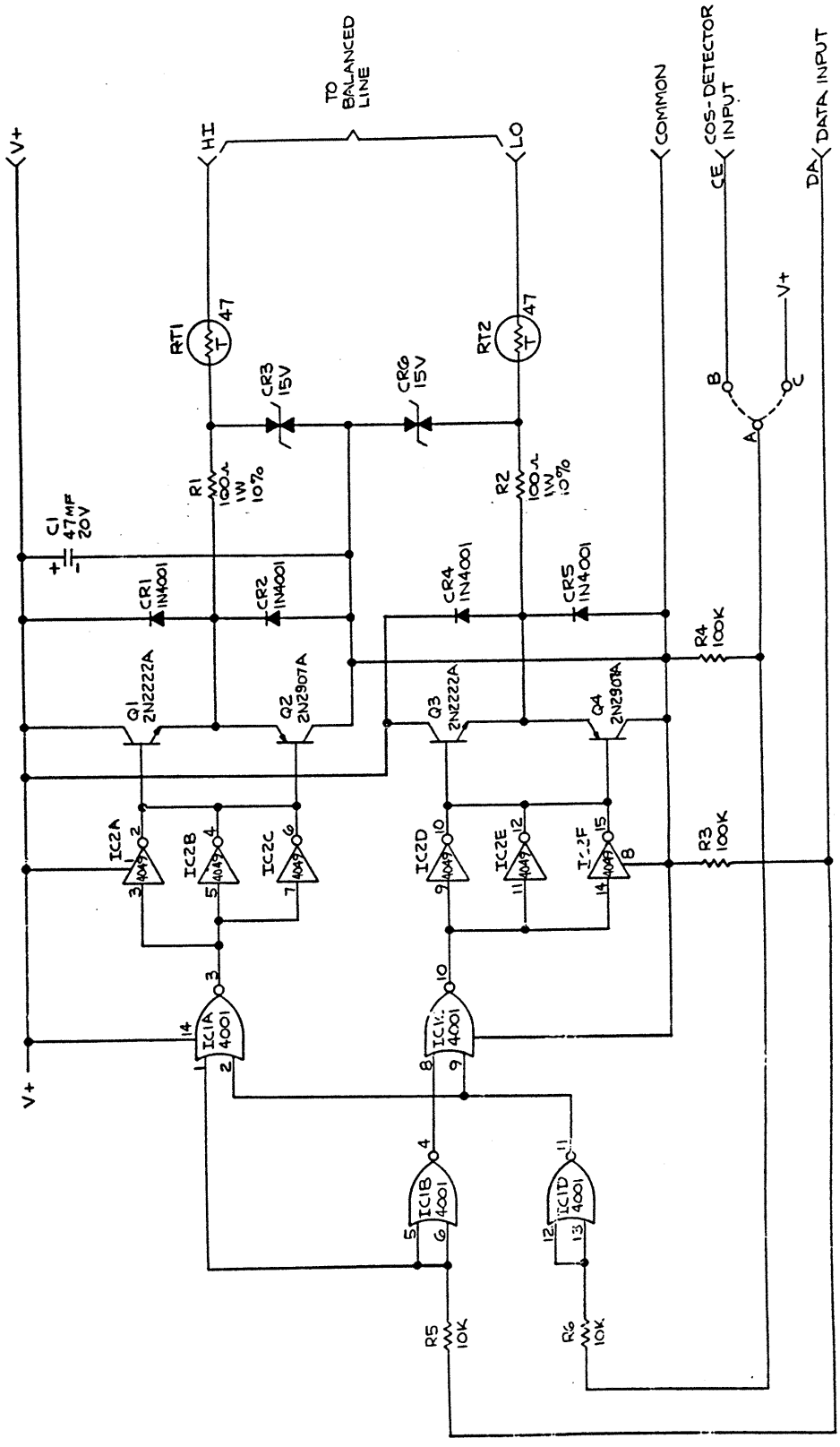

Figure 10. Schematic of circuit for Metallic-Line Driver, Option HB-44980.